

# **PRODUCT SPECIFICATION**

#### Part Number

## PG12232A-O Series

CUSTOMER	
CUSTOMER PART NUMBER	
DESCRIPTION	
APPROVED BY	
DATE	



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## **Record of Revisions**

Rev.	Comments	Page	Date
1	Preliminary Specification was first issued.	All	8/8'14



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# 1. Part number breakdown

Replace each Space (\_) with the following letters and or numbers

1. P-tec LCD Type	C = Character G = Graphic COG = Chip On Glass	COF = Chip On Flex TAB = Tape Automated Bonding TFT = Thin-film Transistor	
2. LCD Model		2002A = 20 Characters x 2 Lines w/ Pins on Left side and 116mm x 37 x 12.7mm overall size 364B = 128 Dots per row x 64 Dots per Column w/ Pins on lower side and 93mm x 70 x 8.8mm overall size	
3. Fluid Type	T = TN/Grey Y = STN/Yellow Green G = STN/ Grey	<ul><li>B = STN/ Blue</li><li>F = FSTN/ White</li><li>N = FSTN/ Black</li></ul>	
4. Backlight/polorizer	NF = None/Transflective NM= None/Transmissive NR=None/Reflective EF= EL/Transflective EM= EL/Transmissive	LF= LED/Transflective LM= LED/Transmissive CF= CCFL/Transflective CM=CCFL=Transmissive	
5. Backlight Color	(If no backlight provided <b>B</b> = Blue/Green <b>Y</b> = Yellow <b>G</b> = Green	move on to viewing angle [6.])  \$ = Yellow/Green  O = Orange  W = White	
6. Viewing Angle	<b>D</b> = 6:00 <b>U</b> = 12:00	R = 3:00 L = 9:00	
7. Internal Number	Single Letter for internal purposes		
8. Extended Temperature	This space is blank if operating temperature is standard 0°C to 50°C An X will be visible if the LCD is Extended operating temperature		
Customer Specials or List of Value-added items	Usually blank unless customer requests some modifications. Can be several Letters long.		

4	P-TEC
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## 2. Precautions in use of LCD Modules

- (1) Avoid applying excessive shocks to the module or making any alterations or modifications to it.
- (2)Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.
- (3)Don't disassemble the LCM.
- (4)Don't operate it above the absolute maximum rating.
- (5)Don't drop, bend or twist LCM.
- (6) Soldering: only to the I/O terminals.
- (7)Storage: please storage in anti-static electricity container and clean environment.

# 3. General Specification

Item	Dimension	Unit	
Number of Dots	122 x 32	_	
Module dimension(No Backlight)	84.0 x 44.0 x 10.0 (MAX)	mm	
Module dimension(With LED Backlight)	84.0 x 44.0 x 14.0 (MAX)	mm	
View area	60.5 x 18.5	mm	
Active area	53.64 x 15.64	mm	
Dot size	0.40 x 0.45	mm	
Dot pitch	0.44 x 0.49	mm	
LCD type	STN		
Duty	1/32		
View direction	6 o'clock or 12 o'clock		
Backlight Type	None, YELLOW-GREEN backlight		



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## 4. Absolute Maximum Ratings

It	tem	Symbol	Min	Max	Unit
Input Voltage		$V_{I}$	-0.3	VDD+0.3	V
Supply Voltage For	Logic	$VDD-V_{SS}$	-0.3	7.0	V
Supply Voltage For	LCD	$V_{DD}$ - $V_0$	Vdd-13.5	0	V
Standard	Operating Temp.	Тор	0	50	$^{\circ}\mathbb{C}$
Temperature LCM	Storage Temp.	Tstr	-10	60	°C
Wide Temperature	Operating Temp.	Тор	-20	70	$^{\circ}\mathbb{C}$
LCM	Storage Temp.	Tstr	-30	80	$^{\circ}$

# 5. Electrical Characteristics

Item	Symbol	Condition	Min	Тур	Max	Unit
Supply Voltage For Logic	$V_{DD}$ - $V_{SS}$	_	4.5	5.0	5.5	V
Supply Voltage For LCD	$V_{DD}$ - $V_0$	Ta=25 ℃	-	6.5	-	V
Input High Volt.	$V_{IH}$	_	$0.7~\mathrm{V_{DD}}$	_	$V_{DD}$	V
Input Low Volt.	$V_{IL}$	_	$V_{SS}$	_	$0.3~\mathrm{V_{DD}}$	V
Supply Current	$I_{DD}$	V <sub>DD</sub> =5V	-	1.0	3.0	mA
Supply Voltage of Yellow-green backlight	$ m V_{LED}$	Forward current =190 mA  Number of LED die 2x19=38	3.8	4.2	4.3	V



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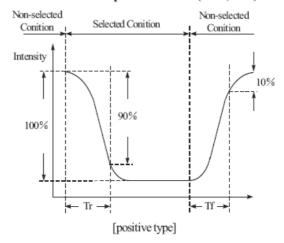
# 6. Optical Characteristics

Item	Symbol	Condition	Min	Тур	Max	Unit
View Angle	(V)θ	CR ≧2	-20	_	35	deg
, te w ringie	(Н)ф	CR≧2	-30	_	30	deg
Contrast Ratio	CR	_	_	3	_	_
Response Time	T rise	_	_	_	250	ms
The species Time	T fall	_	_		250	ms

#### Definition of Operation Voltage (Vop)

# Intensity Non-selected Wave Non-selected Wave Non-selected Wave Cr Max Vop Driving Voltage(V) [positive type]

#### Definition of Response Time (Tr, Tf)

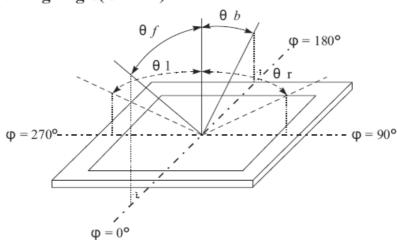


#### Conditions:

Operating Voltage : Vop Viewing Angle( $\theta$ ,  $\phi$ ) :  $0^{\circ}$ ,  $0^{\circ}$ 

Frame Frequency: 64 HZ Driving Waveform: 1/N duty, 1/a bias

## Definition of viewing angle( $CR \ge 2$ )





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# 7. Interface Pin Function

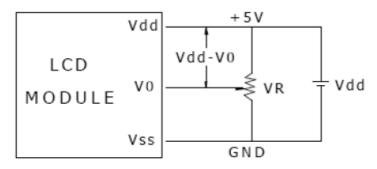
Pin No.	Symbol	Level	Description
1	$V_{SS}$	0V	Ground
2	$V_{DD}$	5.0V	Supply Voltage for logic
3	V0		Operating voltage for LCD
4	A0	H/L	Register Select
5	E1	H/L	Enable For Chip1, Active High, Left Part
6	E2	H/L	Enable For Chip2, Active High, Left Part
7	RW	H/L	Read/Write
8	DB0	H/L	Data bit 0
9	DB1	H/L	Data bit 1
10	DB2	H/L	Data bit 2
11	DB3	H/L	Data bit 3
12	DB4	H/L	Data bit 4
13	DB5	H/L	Data bit 5
14	DB6	H/L	Data bit 6
15	DB7	H/L	Data bit 7
16	RST	H/L	Reset Signal
17	LED(+)		Anode of LED Backlight
18	LED(-)		Cathode of LED Backlight



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## 8. POWER SUPPLY

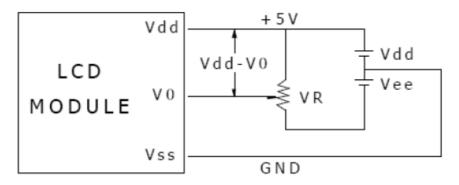
#### SINGLE SUPPLY VOLTAGE TYPE (for LCM with Negative Power on PCB)



Vdd-V0: LCD Driving Voltage

VR: 10K - 20K

## DUAL SUPPLY VOLTAGE TYPE (for LCM without Negative Power on PCB)



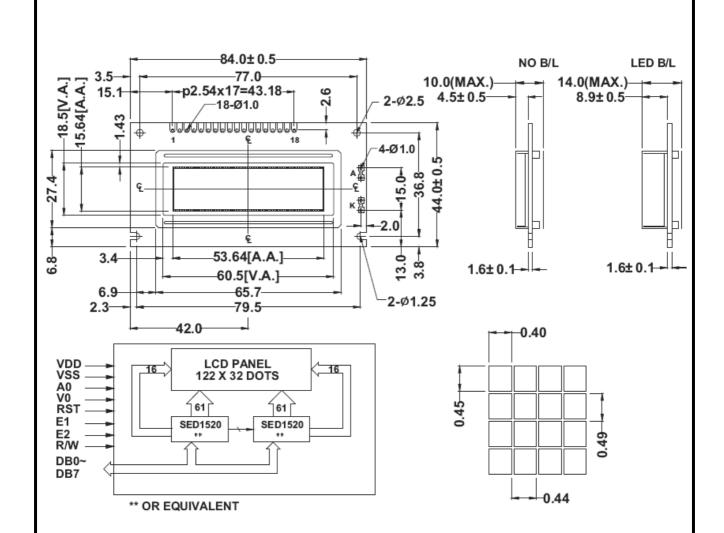
Vdd-V0: LCD Driving Voltage

VR: 10K - 20K



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## 9. Contour Drawing & Block Diagram





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## 10. Timing Characteristics

- AC Characteristics
- Read/Write timing for the 80-port MPU

 $(T_a = -20 \text{ to } 75^{\circ}\text{C}, \text{Vss} = -5.0\text{V} \pm 10\%)$ 

Parameter	Signal	Symbol	Condition		Rating		Unit
rarameter	Signal	Symbol	Symbol Condition		Тур	Max	Offic
Address hold time	A0, CS	tahb		10	_	_	ns
Address set-up time	AU, CS	tawb		20	_	_	ns
System cycle time	WR, RD	tcycs		1000	_	-	ns
Control pulse width	WK, KD	tcc		200	_	-	ns
Data set-up time		tosa		80	_	_	ns
Data hold time	D0 ~ D7	tDH8		10	_	_	ns
RD access time		taccs	CL = 100pF	_	_	90	ns
Output disable time	] ]	tонв	OL - 100pi	10	_	60	ns

<sup>\*2.</sup> The ratings when Vss = -3.0V are approximately 100% higher than when Vss = -5.0V.

#### Read/Write timing for the 68-port MPU

 $(T_a = -20 \text{ to } 75^{\circ}\text{C}, \text{Vss} = -5.0\text{V} \pm 10\%)$ 

Parameter		Signal	Symbol	Condition	Rating			Unit	
Faramete	=1	Signal	Symbol	Symbol Condition		Тур	Max	Offic	
System cycle tim	ne	A0, CS	tcyce *3		1000	_	_	ns	
Address set-up t	ime	R/W	tawe		20	١	1	ns	
Address hold tim	ne	I IVVV	tане		10			ns	
Data set-up time			tose		80	_	_	ns	
Data hold time		D0 ~ D7	tрне		10	_	-	ns	
Output disable ti	me	00.07	tоне	C <sub>L</sub> = 100pF	10	_	60	ns	
Access time			tacce	OL - 100pi	_	-	90	ns	
Enable pulse	READ	Е	tew		100	_	_	ns	
width	WRITE	_	iew		80	_	_	ns	

<sup>\*3.</sup> tcycs indicates the cycle during which CS/E are HIGH: it does not indicate the cycle of the E signal.

#### Control timing for 80-port/68-port display

 $(T_a = -20 \text{ to } 75^{\circ}\text{C}, \text{Vss} = -5.0\text{V} \pm 10\%)$ 

Parameter	Signal	Symbol	ool Condition		Rating		
raiailletei	Signal	Symbol	Condition	Min	Тур	Max	Unit
LOW pulse width		twLCL		35	_	_	μs
HIGH pulse width	CL	twncl		35	_	_	μs
Rising time	OL	tr		_	30	150	ns
Falling time	]	tr		_	30	150	ns
FR delay time	FR	torr	(Input timing)	-2.0	0.2	2.0	116
I I delay tille	''K	LUFK	(Output timing), CL = 100pF	_	0.2	0.4	μs

<sup>\*5.</sup> The ratings when  $\forall$ ss = -3.0 $\forall$  are approximately 100% higher than when  $\forall$ ss = -5.0 $\forall$ .

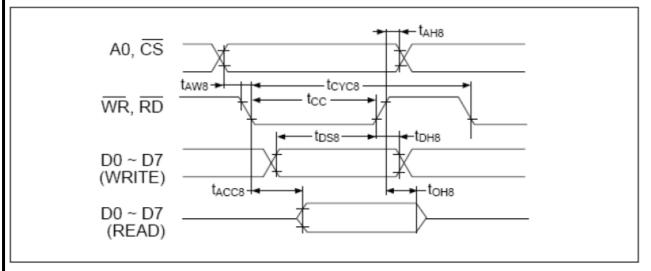
<sup>\*4.</sup> The ratings when Vss = -3.0V are approximately 100% higher than when Vss = -5.0V.

<sup>\*6.</sup> The input timing of the FR delay time is determined by the SED1520 (Slave). The output timing of the FR delay time is determined by the SED1520 (Master).

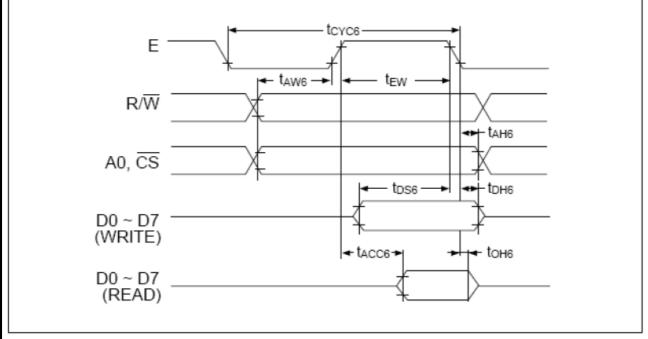


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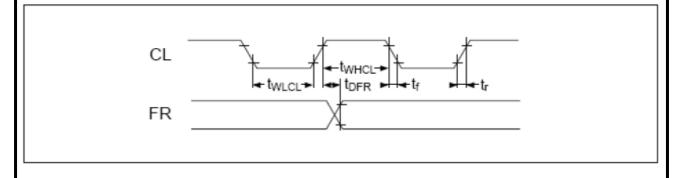
- Timing Chart
   Read/Write timing for the 80-port MPU



o Read/Write timing for the 68-port MPU



o Control timing for 80-port/68-port display





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# **11.Instruction Table**

# ■ DISPLAY COMMANDS (Based on the 80-port MPU; the RD and WR commands differ for the 68-port MPU.)

1 Display ON/OFF 1 0 0 0 1 0 1 0 1 1 1 0 0 1 1 0 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0	Г	Command RDWR A0 D7 D6 D5 D4 D3 D2 D1 D0 Function													
Display ON/OFF  Display START Line  Display START Line  Display START Line  Display START Determines the line of RAM data to be displayed at address (0~31) display's top line (COM0).  Regal Address Set  Display START Determines the line of RAM data to be displayed at address (0~31) display's top line (COM0).  Column (Segment) Address Set  Column address Sets the page of the Display RAM in the page address register.  Reads the status. BUSY 1: Busy (internal processing) 0: READY stat	4						_	4	_						N or OFF, regardless of the
2   Line	1	Display ON/OFF	1	U	U	1	U	1	U	1	1	1	0/1		
Line	_	Display START	4	_	^	4	4	_	Dis	pla	ıy S	ST/	RT	Determines the line of RAM	I data to be displayed at the
4 Column (Segment) 4 Column (Segment) 5 Status Read 6 Write Display Data 7 Read Display Data 8 ADC Select 1 0 0 1 0 1 0 1 0 1 0 0 0 0 0 0 0 0 0 0	4	Line	1	U	U	1	1	U	ado	dre	ss	(0~	31)	display's top line (COM0).	
4 Column (Segment) Address Set	2	Dago Addrose Sot	1	٥	n	1	۸	1	1	1	٥	Pa	age	Sets the page of the Displa	y RAM in the page address
Address Set   1 0 0 0		rage Address Set	<u>'</u>	U	U	<u>'</u>	U	'	'	_	U	(0	~3)	register.	
Address Set	4	Column (Segment)	1	0	n	٥		Col	um	n a	ddr	es	s	Sets the column address of the	ne Display RAM in the column
Status Read  O 1 0 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	Ľ	Address Set	Ľ		_	Ŭ			(0	~7	9)			address register.	
Status Read  O 1 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0														Reads the status.	
ON/OFF 1: Display OFF								ш	_					BUSY 1: Busy (internal pr	rocessing) 0: READY status
ON/OFF 1: Display OFF	5	Status Read	ln	1	n	š	ပ္ပ	P	SET	n	0	0	0	ADC 1: Rightward (forw	ard) output
RESET 1: Resetting 0: Normal Write Display Data 1 0 1 Write Data Writes the data on the data bus to RAM Read Display Data 0 1 1 Read Data Read Data RAM onto the data bus. These commands access previously-specified address of the Display RAM onto the data bus.  Read Display Data 0 1 1 Read Data Read Data RAM onto the data bus. These commands access previously-specified address of the Display RAM onto the data bus.  Read Display Data 0 1 1 Read Data RAM onto the data bus. These commands access previously-specified address of the Display RAM onto the data bus.  Used to reverse the correspondence between the Display RAM's column addresses and segment driver output p 0: Rightward (forward) output 1: Leftward (reverse) output p 0: Rightward (forward) output 1:	ľ	Cidido Neda	ľ		٠	8	Ä	Š	RE	٠	Ü			0: Leftward (revers	se) output
Write Display Data 1 0 1 Write Data Writes the data on the data bus to RAM Reads data from the Display Address of the Display RAM onto the data bus.  Read Display Data 0 1 1 Read Data Read Data Read Data Reads data from the Display RAM onto the data bus.  Back and Display Data 0 1 1 Read Data Read Data Reads data from the Display RAM onto the data bus.  Back and Display Data 0 1 1 1 Read Data Read Data RAM onto the data bus.  Back and Display Data 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1								Ĭ						ON/OFF 1: Display OFF	0: Display ON
bus to RAM Reads data from the Display Data   1 0 1   Read Data   Reads data from the Display   Readfress of the Display RAM onto the data bus.   Read Data   Reads data from the Display   RAM onto the data bus.   Read Data   Reads data from the Display   RAM onto the data bus.   Read Data   Reads data from the Display RAM onto the data bus.   Read Data   Reads data from the Display RAM onto the data bus.   Read Data   Reads data from the Display RAM onto the data bus.   Read Data   Reads data from the Display RAM onto the data bus.   Read Data   Reads data from the Display RAM onto the data bus.   Read Data   Reads data from the Display RAM onto the data bus.   Read steep in the Display RAM onto the data bus.   Reads data from the Display RAM onto the data bus.   Reads data from the Display RAM onto the data bus.   Reads data from the Display RAM onto the data bus.   Reads steep in the Display RAM onto the Display RAM o														RESET 1: Resetting	0: Normal
Read Display Data 0 1 1 Read Data Read Data Read Sata from the Display address of the Display RAM onto the data bus.    Read Display Data   Read Data   Read Data   Read Sata from the Display RAM onto the data bus.   Read Data   Read D	6	Write Display Data	1	0	1			w	rito	Da	nta			Writes the data on the data	These commands access a
Read Display Data 0 1 1 Read Data RAM onto the data bus. after which the column dress is incremented by a series of the column dress is incremented by a series of the column addresses and segment driver output processes and segment driver output	ľ	Write Display Data	ļ '	U	'			**	IIIC	Da	itea			bus to RAM	previously-specified
dress is incremented by a Used to reverse the correspondence between the Disp Used to reverse the column address counter to 0 and page Used to reverse the column address counter to 0 and page Used to reverse the column address counter to 0 and page Used to reverse the column address counter to 0 and page Used to reverse the column address counter to 0 and page Used to reverse the column address counter to 0 and page Used to reverse the column address counter to 0 and page Used to reverse the column address counter to 0 and page Used to reverse the column address counter to 0 and page Used to reverse the column address counter to 0 and page Used to reverse the column address counter to 0 and page Used to reverse the column address counte	Г													Reads data from the Display	address of the Display RAM,
Used to reverse the correspondence between the Display ADC Select    1	7	Read Display Data	0	1	1			Re	ead	Da	ıta			RAM onto the data bus.	after which the column ad-
8 ADC Select 1 0 0 1 0 1 0 0 0 0 0 0/1RAM's column addresses and segment driver output p 0: Rightward (forward) output 1: Leftward (reverse) output p 0: Rightward (forward) output 1: Leftward (reverse) output p 0: Rightward (forward) output 1: Leftward (reverse) output p 0: Rightward (forward) output 1: Leftward (reverse) output p 0: Rightward (forward) output 1: Leftward (reverse) output p 0: Rightward (forward) output 1: Leftward (reverse) output p 0: Rightward (forward) output 1: Leftward (reverse) output p 0: Rightward (forward) output 1: Leftward (reverse) output p 0: Rightward (forward) output 1: Leftward (reverse) output p 0: Rightward (forward) output 1: Leftward (reverse) output p 0: Rightward (forward) output 1: Leftward (reverse) output p 0: Rightward (forward) output 1: Leftward (reverse) output p 0: Rightward (forward) output 1: Leftward (reverse) output p 0: Rightward (forward) output 1: Leftward (reverse) output p 0: Rightward (forward) output 1: Leftward (reverse) output p 0: Rightward (forward) output 1: Leftward (reverse) output p 0: Rightward (forward) output 1: Leftward (reverse) output p 0: Rightward (forward) output 1: Leftward (reverse) output 1: Leftward (reverse															dress is incremented by one.
9 Static Drive ON/OFF 1 0 0 1 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 0 1 0														Used to reverse the correspo	ndence between the Display
Static Drive ON/OFF  1 0 0 1 0 1 0 0 1 0 0 1 0 0/1display operation. 1: Static drive (Power Save) *7 0: Normal drive driv	8	ADC Select	1	0	0	1	0	1	0	0	0	0	0/1	RAM's column addresses and	d segment driver output ports
9 ON/OFF 1 0 0 1 0 1 0 0 1 0 0 1 0 0/1 display operation. 1: Static drive (Power Save) *7 0: Normal display operation. 1: Static drive (Power Save) *7 0: Normal display operation. 1: Static drive (Power Save) *7 0: Normal display operation. 1: 1/32 duty 0: 1/16 duty 1: 1/32 duty 0: 1/16 duty 1: 1/32 duty 0: 1/16 duty 1: Increments the column address counter by one only will display data is written but not when it is read. 1: Increments the column address counter by one only will display data is written but not when it is read. 1: Increments the column address counter by one only will display data is written but not when it is read. 1: Increments the column address counter by one only will display data is written but not when it is read. 1: Increments the column address counter by one only will display data is written but not when it is read. 1: Increments the column address counter by one only will display data is written but not when it is read. 1: Increments the column address counter by one only will display data is written but not when it is read. 1: Increments the column address counter by one only will display data is written but not when it is read. 1: Increments the column address counter by one only will display data is written but not when it is read. 1: Increments the column address counter by one only will display data is written but not when it is read. 1: Increments the column address counter by one only will display data is written but not when it is read. 1: Increments the column address counter by one only will display data is written but not when it is read. 1: Increments the column address counter by one only will display data is written but not when it is read. 1: Increments the column address counter by one only will display data is written but not when it is read. 1: Increments the column address counter by one only will display data is written but not when it is read. 1: Increments the column address counter by one only will display data is written but not when it is read. 1: Increments t														0: Rightward (forward) output	1: Leftward (reverse) output
9 ON/OFF 1 0 0 1 0 1 0 0 1 0 0 1 0 0/1display operation. 1: Static drive (Power Save) *7 0: Normal display opera  10 Duty Select 1 0 0 1 0 1 0 1 0 0 0/1  Read Modify Write 1 0 0 1 1 1 0 0 0 0 0 0  Increments the column address counter by one only widesplay data is written but not when it is read.  12 End 1 0 0 1 1 1 0 0 1 1 1 0 0 0 1 0 0 Resets the Display START line to the 1st line in the register.  13 Reset 1 0 0 1 1 1 1 0 0 0 1 0 0 Resets the column address counter to 0 and page		Static Drive												Selects normal display ope	ration or static all-lit drive
10 Duty Select 1 0 0 1 0 1 0 1 0 0 0 0 0 Selects the duty factor for driving LCD cells. 1: 1/32 duty 1: 1/32	9		1	0	0	1	0	1	0	0	1	0	0/1	display operation.	
10 Duty Select	L	010011												1: Static drive (Power Save) *7	0: Normal display operation
1: 1/32 duty 0: 1/16 duty  11 Read Modify Write 1 0 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0	10	Duty Select	1	0	n	1	0	1	0	1	0	٥	0/1	Selects the duty factor for d	Iriving LCD cells.
11   Read Modify Write   1	Ľ	Daty Colect	Ľ		J	Ľ								*	,
display data is written but not when it is read.  12 End  1 0 0 1 1 1 0 0 1 1 1 0 Cancels the Ready Modify Write mode.  Resets the Display START line to the 1st line in the register.  13 Reset  1 0 0 1 1 1 0 0 0 1 0 Resets the column address counter to 0 and page.	11	Read Modify Write	1	0	n	1	1	1	0	0	0	0	n	Increments the column addre	ss counter by one only when
Resets the Display START line to the 1st line in the register 13 Reset 1 0 0 1 1 1 0 0 0 1 0 Resets the column address counter to 0 and page		-												' '	
13   Reset	12	End	1	0	0	1	1	1	0	1	1	1		, ,	
															I
address register to 3	13	Reset	1	0	0	1	1	1	0	0	0	1	0	Resets the column address	counter to 0 and page
address register to 5.														address register to 3.	

<sup>\*7.</sup> Power Save mode is entered by selecting static drive in Display OFF status.



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# 12.Quality Assurance

#### Screen Cosmetic Criteria

Item	Defect	Judgment Criterion	Partition
1	Spots	A)Clear	Minor
2	Bubbles in Polarizer		Minor
3	Scratch	In accordance with spots cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.	Minor
4	Allowable Density	Above defects should be separated more than 30mm each other.	Minor
5	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels.  Back-light type should be judged with back-light on state only.	Minor



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# 13.Reliability

### Content of Reliability Test

Environmental	Environmental Test						
Test Item	Content of Test	Test Condition	Applicable Standard				
High Temperature storage	Endurance test applying the high storage temperature for a long time.	60℃ 96hrs					
Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-10℃ 96hrs					
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	50°C 96hrs					
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	0℃ 96hrs					
High Temperature/ Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time.	60℃,90%RH 96hrs					
High Temperature/ Humidity Operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	50℃,90%RH 96hrs					
Temperature Cycle	Endurance test applying the low and high temperature cycle.  -10°C 25°C 60°C  30min 5min 30min 1 cycle	-10°C/60°C 10 cycles					
Mechanical Test							
Vibration test	Endurance test applying the vibration during transportation and using.	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hrs					
Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G Half sign wave 11 msedc 3 times of each direction					

<sup>\*\*\*</sup>Supply voltage for logic system=5V. Supply voltage for LCD system=Operating voltage at  $25^{\circ}$ C